ABSTRACT OF THE DISCLOSURE

A signal delay compensating circuit which is a digital circuit includes: a first semiconductor circuit device (100) having a clock-signal generating circuit (1) and a data processing circuit (2) and adapted to output a data signal in synchronism with a clock signal; and a second semiconductor circuit device (4) to which the output data signal is inputted and which processes the input data signal in synchronism with the clock signal. The clock signal to be supplied from the first semiconductor circuit device (100) to the second semiconductor circuit device (4) is fed back to the data processing circuit (2), and the fed-back clock signal is used as a clock signal at the time of outputting the data signal. A signal delay compensating circuit which effects compensation by following the delay of a reference signal is thereby provided.